

Meeting challenges for engineering the gate stack

OVERVIEW

Precise interfacial layer control and film compositional control are needed to extend SiON layers with high nitrogen content for 32nm node high-performance (HP) logic devices, as well as when Hf-based films at the 65nm node are introduced for low standby-power (LSTP) logic devices. Using XPS and EM-probe analysis, quick, full-wafer mapping of chemical composition and electrical gate-leakage characteristics of both the gate dielectric film and interfacial layer are possible. Atomic vapor deposition (AVD) achieves hafnium-based gate dielectrics with the precision of ALD at the throughput of MOCVD. Ge-channel formation by infusion doping could provide the channel-mobility improvements needed for continued CMOS scaling without using Ge wafers.

SiON gate dielectrics can be extended to the 32nm node for HP and 45nm-node low operating-power (LOP) logic devices through nitrogen composition engineering in the 30–40% level to achieve a k value above 6, as demonstrated through a nitride/oxide stack structure. This level of nitrogen compositional control reduces gate leakage by three to four orders-of-magnitude compared to SiO₂. LSTP logic devices require four orders-of-magnitude reduction in gate leakage at the 65nm node, which is right at the limit for SiON with a k value of 7. Therefore, some companies will introduce Hf-based dielectrics such as HfSiON with a k value between 9 and 11. At the 32nm node, LSTP logic devices require five orders-of-magnitude reduction in gate leakage, necessitating k values >20 with much higher Hf content and no more than two monolayers of interfacial oxide layer.

Extending SiON to the sub-45nm node

The industry switched from pure SiO₂ gate dielectric to lightly nitrated oxides for logic devices as the gate thickness scaled below 2.2nm at the 180nm node to prevent boron penetration from the p+ poly-gate electrode using thermal nitridation of oxide (TN-O). Pure SiO₂ has a k value of 3.9; however, heavy doping with nitrogen increases the k value toward Si₃N₄ ($k = 7.8$) and reduces gate leakage (Fig. 1) [1].

Today, heavily nitrogen-doped oxynitrides (SiON) used through the 90nm node are formed by either thermal nitridation (TN-O) or plasma nitridation (PN-O) of an SiO₂ oxide layer with nitrogen

compositional engineering up to a few percent. Nitrogen pile-up at the SiO₂/Si interface is observed with TN-O, while no pile-up occurs with PN-O, but plasma-induced surface damage has been reported and must be avoided [2]. However, Ludsteck et al. just reported high nitrogen-content SiON films >50% grown by rapid

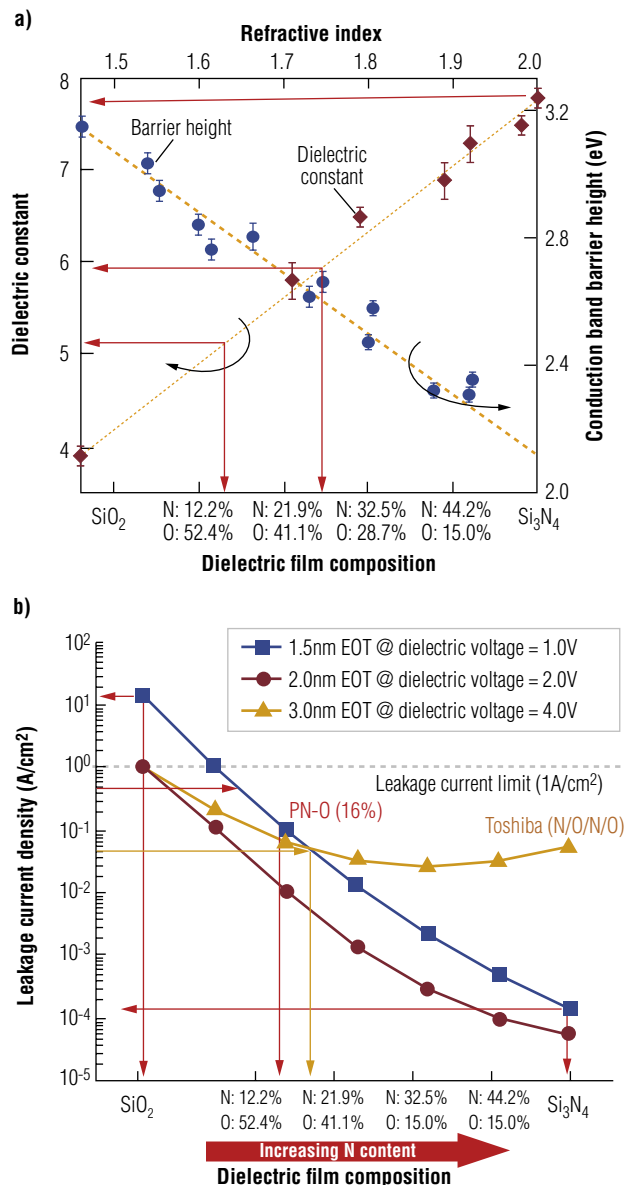


Figure 1. Influence of nitrogen content on a) dielectric constant (k value) and b) leakage current [3].

John Borland, J.O.B. Technologies, South Hamilton, Massachusetts; Emir Gurer, ReVera Inc., Sunnyvale, California; Mark Benjamin, Solid State Measurements Inc., Pittsburgh, Pennsylvania; Wes Skinner, Epion Corp., Billerica, Massachusetts; Tom Seidel, Genus Inc., Sunnyvale, California; Marcus Schumacher, Aixtron AG, Aachen, Germany

thermal nitridation (RTN) without N pile-up and four orders-of-magnitude reduction in gate leakage. Increasing the nitrogen doping content to 16% increases the k value to 5.5 and reduces gate leakage by 30× [3]. This is close to the 100× improvement shown in **Fig. 1b** (0.3A/cm² vs. 0.15A/cm²) [1].

Also, SiON with 30% nitrogen has a k value of 6 and a ~1000× reduction in gate leakage (I_G), as shown in **Fig. 1b** [3]. These high levels of N concentration can be achieved using either an oxide/nitride (O/N) or nitride/oxide (N/O) stack dielectric structure in combination with re-oxidation and/or re-nitridation processing steps.

Blosse et al. reported a 10× reduction in I_G for an N/O stack structure compared to TN-O [4]. Matsushita et al. also reported using a re-nitrided, oxidized nitride stack structure (N/O/N/O) to reduce I_G by three orders-of-magnitude compared to SiO₂, achieving a 0.75nm equivalent oxide thickness (EOT) with $I_G = 92A/cm^2$ that satisfies 45nm-node HP logic devices, with possible extension to the 32nm node [5]. The authors reported that SiO₂ has excellent interfacial properties but a low dielectric constant ($k = 3.9$) and poor gate leakage, while Si₃N₄ has poor interfacial properties but higher dielectric constant ($k = 7.8$) and excellent gate leakage (three to five orders-of-magnitude reduction). Referring to **Fig. 1b**, this N/O/N/O stack structure would correspond to a N content >19% and 300× reduction in leakage.

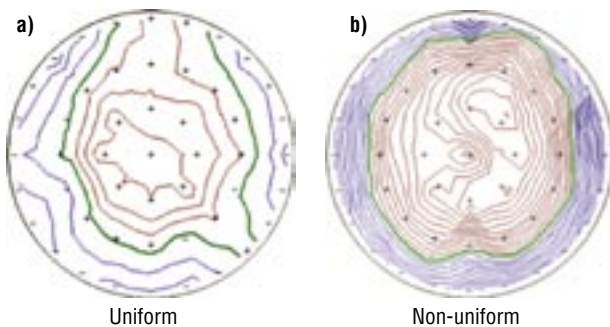


Figure 2. Comparison of SiON **a)** thickness uniformity (15Å at <1.0% uniformity) to **b)** compositional uniformity (1.1×10¹⁵ atoms/cm² at 8.66% uniformity).

The ideal SiON stack structure, therefore, is ALD Si₃N₄ (0.8nm)/two monolayers of low-temperature (600°C) thermal oxide (<0.4nm)/Si substrate for an EOT of <0.8nm. Since $EOT = T_{SiON}(3.9/k)$ to achieve an $EOT = 0.7nm$, if $k = 5$, then $T_{SiON} = 0.89nm$; if $k = 6$, then $T_{SiON} = 1.07nm$; and if $k = 7$, then $T_{SiON} = 1.25nm$. Bohr reported that Intel will not scale its SiON gate below an EOT of 1.2nm going from the 90nm node to the 65nm node due to gate-leakage constraints at 100A/cm², keeping the overall chip power at tolerable levels [6]. Other HP logic companies also say they will extend SiON dielectrics below the 45nm node [7].

SiON film characterization

The key to extending SiON is precise N compositional control. A 49-point wafer mapping by x-ray photoelectron spectroscopy (XPS) for a 1.5nm SiON gate is shown in **Fig. 2**. The SiON film-thickness uniformity was good at <1% (**Fig. 2a**), but the N compositional uniformity was poor at 8.66%, as shown in **Fig. 2b**. N compositional variation across the wafer due to the PN-O process directly correlates to device threshold-voltage (V_t) variation across the wafer. It was determined that the sensitivity of N content on V_t for pMOS devices is 45mV/%N and for nMOS devices is 15mV/%N [8].

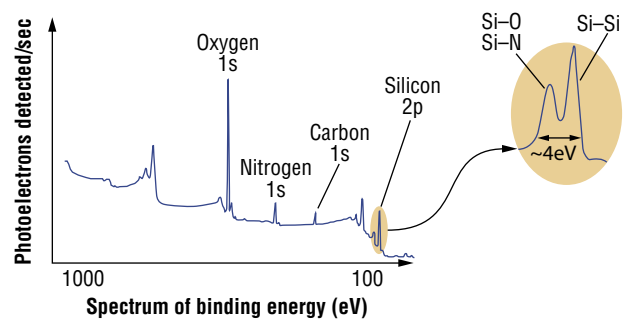


Figure 3. Spectrum of SiON from in-line XPS metrology system.

Good linearity between initial oxide thickness and increasing N content (dose) was also observed, but the slopes of the lines were different. Using a plasma nitridation system for control doping with nitrogen, a 4×10¹⁵/cm² dose of N increased the thickness by 0.8nm for a 0.55nm-thick initial oxide wafer, while a 1.6nm-thick initial oxide wafer had an increase of only 0.4nm.

Metrology technology overview

The wafer maps of composition measurements were made with a new, in-line, compositional metrology system based on XPS, which device makers are rapidly adopting. Used in the laboratory for decades, XPS has emerged as the optimal method for measuring semiconductor ultrathin films for thickness and composition. The present tool is an automated and recipe-driven in-line metrology system.

XPS is conceptually very simple. Low-energy x-rays illuminate a surface, penetrating it to a few microns in depth. The atoms comprising the material absorb the x-rays, and in many cases the atom will eject an electron. The electron is emitted with an energy that is proportional to the binding energy of the electron to the atom. Because the binding energy is a characteristic of the atom and its chemical state, measuring the number of electrons at a specific energy will provide the fundamental composition information of the material.

A typical SiON spectrum is depicted in **Fig. 3**. Photoelectrons from Si are at a binding energy near 100eV. This region contains information from Si atoms in the substrate Si as well as from Si in the film, separated by the difference in binding energy states of atoms in those different chemical states. Nitrogen, oxygen, and carbon are also contained in the measured spectrum. From these spectral features, the composition and thickness of the film can be determined.

Rapid gate-leakage measurements can be achieved using special elastic material probes, called EM-probes. This technique uses an EM-probe to make a temporary electrical contact to the film of interest, allowing immediate measurement of electrical data without having to wait until final test. A different version of the probe is separately opti-

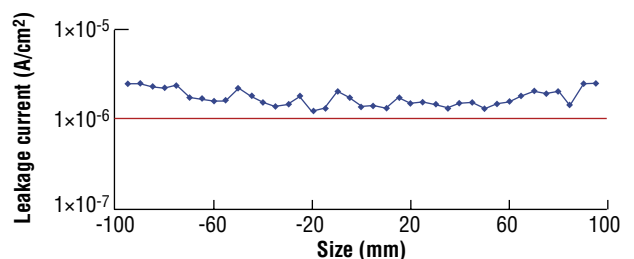


Figure 4. Thirty-nine-point EM-probe gate-leakage diameter scan showing 3× leakage variation.

Gate leakage roadmap						
Technology node (nm)	HP		LOP		LSTP	
	EOT (nm)	I_G (A/cm ²)	EOT (nm)	I_G (A/cm ²)	EOT (nm)	I_G (A/cm ²)
90	1.2	4.5×10^2	1.5	2	2.1	5.1×10^{-3}
65	0.95	9.3×10^2	1.2	5	1.6	2.3×10^{-2}
45	0.75	1.9×10^3	0.9	11	1.4	8.0×10^{-2}
32	0.6	7.7×10^3	0.8	21	1.1	0.14
22	0.5	1.9×10^4	0.7	91	1.0	0.25
Hf-based dielectric needed						

mized for capacitance voltage measurements.

Good correlation with MOS transistors was demonstrated by Olsen et al. [9]. Both wafer-mapping and diameter-scan measurements are possible with the EM-probe technique; a 39-point diameter scan is shown in Fig. 4 for a PN-O film with an EOT = 1.3nm, where a 3× variation in I_G was observed between $1\text{--}3 \times 10^{-6}$ A ($0.05\text{--}0.15$ A/cm²). This could represent a N content fluctuation from 13–18% derived from Fig. 1b.

Hf-based gate dielectrics

Pure HfO₂ has a k value of 26, and depending on the interfacial-oxide layer thickness, a five to nine orders-of-magnitude reduction in gate leakage compared to SiO₂ can be achieved. The most promising high- k dielectric material for the industry is Hf-based, and the k value varies from a low of 6 to a high of 26 depending on the film's Hf content and other impurities. For example, nitrided Hf silicate (HfSiON) has a k value from 9–11. The relationship between EOT, dielectric thickness (T_d), and dielectric constant (k) is shown below.

$$\text{EOT} = T_{\text{interfacial oxide}} + \text{EOT}_{\text{high-}k} \quad \text{where} \quad \text{EOT}_{\text{high-}k} = T_d(3.9/k) \quad (1)$$

An EOT of 1.4nm is the target for the 45nm-node LSTP application; 0.9nm is the target for LOP. If the interfacial oxide is kept at 0.8nm to maintain good channel/surface mobility, that leaves $\text{EOT}_{\text{high-}k} = 0.6$ nm and 0.1nm for LSTP and LOP applications, respectively. With a k value of 10, $T_{\text{high-}k} = 1.5$ nm and 0.26nm for LSTP and LOP applications, respectively; if $k = 20$, then $T_{\text{high-}k} = 3.0$ nm and 0.52nm, respectively. So very thin HfSiON films with

excellent compositional control are required. Because the deposition thickness is 0.07nm/cycle, the 1.5nm HfSiON film could be formed by MOCVD or ALD (~21 ALD cycles), while the 0.26nm film would require four ALD cycles.

From the 2003 ITRS, the targeted EOTs and gate leakages for HP, LOP, and LSTP logic devices are listed in the table for the 90–22nm nodes [10].

Hf-based gate dielectrics will first be introduced at 65nm in 2006 for LSTP logic devices in Japan, in order to achieve an EOT of 1.6nm with an I_G of $<2.3 \times 10^{-2}$ A/cm². This can be accomplished with HfSiON or HfSiO deposited by PVD, MOCVD, or ALD, though there are concerns regarding surface damage using the PVD technique.

There also have been contradictory reports when comparing MOCVD and ALD Hf-based films. Some researchers at Selete have reported no differences between MOCVD HfSiON and ALD HfAlO films [11], while others at Selete have shown up to 10× improvement in I_G when switching from MOCVD to ALD for HfSiON [12]. A possible explanation for this is the Hf and Si source materials used for the work. Selete also reported a 100× reduction in I_G when switching from HfCl to Hf-TEMA for HfAlO films [13]. An additional 10× reduction in I_G was observed for ALD HfAlO by eliminating the N content [14]. Kim et al. of Samsung reported excellent carrier mobilities and I_G value of 5×10^{-3} A/cm² at 1.3nm EOT

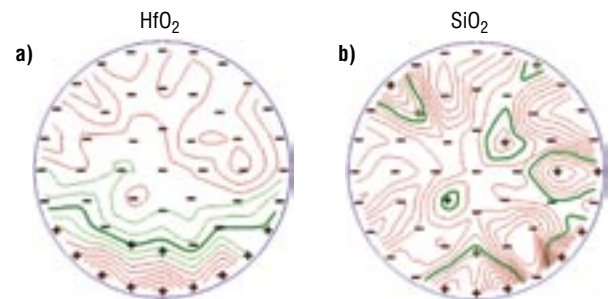


Figure 6. XPS analysis of a) a 4.5nm HfO₂ film and b) a thin 0.43nm interfacial oxide layer.

with ALD HfSiO films, engineering the sequencing between Hf and Si chemical precursors [15].

For low Hf-content films, and thus a low k value, the Hf-dielectric film thickness will be between 1–2nm; therefore, precise control of deposition is required for compositional control. Ideally, ALD control with CVD rates is desired. This has been achieved using a new MOCVD technique called AVD. Typically, this results in linear deposition of HfO₂ at 0.06nm/injection pulse every 1/3 of a second for a deposition rate of 0.18nm/sec. Varying the pulse ratio of the precursors changes the Hf composition in the film. Results from using this AVD technique to deposit Hf films with k values of 6, 11, 14, and 20 with films of 21%, 44%, 70%, and 100% Hf are shown in Fig. 5 for leakage vs. EOT. For an EOT of 2nm, increasing the Hf content from 21% to 100% reduces leakage by more than four orders-of-magnitude [16].

One of the critical issues in scaling Hf-based dielectrics is reducing the interfacial oxide layer without degrading surface channel mobility. This interfacial oxide layer can dominate gate-leakage degradation as EOT scales below 1.2nm for these Hf-based oxides. Using in situ hydrogen baking prior to high- k (ZrO) deposition

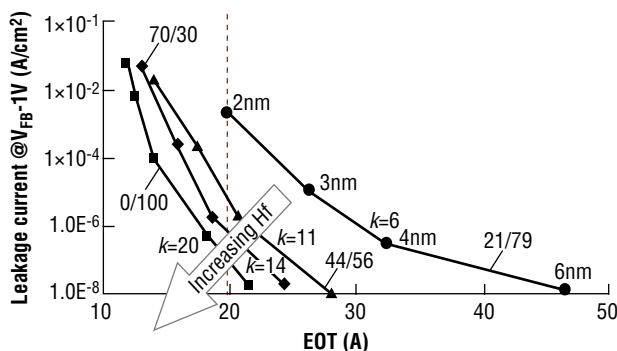


Figure 5. Increasing Hf content (21–100%) and k value (6–20) to reduce leakage and scale EOT [15].

totally eliminated the interfacial oxide, realizing a 0.4nm EOT with $<1 \times 10^{-10} \text{A/cm}^2$ I_G [17]. Without this interfacial oxide layer, however, a delay in deposition/growth and spotty nucleation for both MOCVD and ALD Hf-based films occurs [18, 19].

Besides limiting EOT scaling, the interfacial oxide layer also affects channel mobility; reducing the interfacial oxide from 1.2nm to 0.8nm thereby reduces mobility by a factor of two from $150 \text{cm}^2/\text{Vs}$ to $75 \text{cm}^2/\text{Vs}$ [20]. This sandwiched interfacial-oxide layer can easily be characterized by XPS in a single measurement, as illustrated in Fig. 6 for a 4.5nm HfO_2 film with a 0.43nm interfacial oxide layer. Therefore, XPS can be used to measure the thickness and composition of multilayer stack structures due to the high information content in the spectra of most films. The sensitivity to ultrathin interfacial layers is one key application of this capability.

In XPS, film thickness is determined by observing the attenuation of photoelectron intensities. In a single-layer film on a Si substrate, the thickness of the film can be quantified by observing the loss of photoelectron signal from the Si substrate's Si atoms. The attenuation is a function of the thickness and composition of the material above the substrate. Once the constituent atoms in the overlayers are determined (via XPS), the thickness is determined by applying a physical model. This attenuation behavior is a well understood and invariant physical phenomenon.

Channel-mobility enhancements

As mentioned earlier, the use of high- k gate dielectrics results in

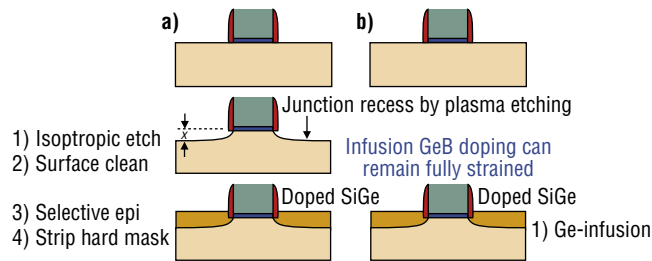


Figure 7. Improving pMOS mobility through SiGe for SDE by a) SEG or b) Ge-infusion doping.

severe channel-mobility degradation because the interfacial-oxide layer thickness is reduced. Therefore, along with the introduction of Hf-based gate dielectrics, channel-mobility enhancement techniques are required. A few years ago, the industry was excited about global strained Si on SiGe epitaxy, but that has disappeared primarily because its benefits diminish as L_g scales below $0.2 \mu\text{m}$ [21]. Other reasons include costs, defect levels, strain durability, and incompatibility with pMOS devices, driving the industry to adopt various localized, process-induced strained-Si techniques instead.

The desired strain directions for nMOS are biaxial-tensile, while for pMOS they are uniaxial-compressive. So starting at the 90nm node, the industry used the shallow-trench isolation device structure to induce compressive strain; nitride-capping layers around the gate stack structures to induce tensile and/or compressive strain; and selective SiGeB epi elevated source/drain structures to induce compressive strain in the channel for pMOS devices [21]. Improved versions of these various techniques and their combinations will continue to be used for the 65nm and 45nm nodes. Figure 7 shows two new approaches that improve the compressive strain in the channel for pMOS devices using SiGeB for source/drain

extension (SDE) formation by either selective epi growth (SEG) or Ge-infusion doping [22, 23]. This replaces traditional ultralow-energy boron implantation because boron doping is included with the SiGe deposition or infusion process. There are limits, however, to using localized strained-Si techniques to improve channel mobility beyond 1.5 \times , but the 2003 ITRS states that an improvement $>2\times$ will be needed by 2007 [10]. For this reason, the industry has begun studying Ge CMOS devices to take full advantage of the potential 2.6 \times improvement in electron mobility and 4.2 \times improvement in hole mobility [24].

Results for gate-dielectric leakage on Ge wafers are similar to Si as reported in [17]: The film without an interfacial layer has the lowest gate leakage, but there are some other issues if the interfacial layer is missing [25]. GeO_2 is soluble in water and GeO_x will desorb from the surface at low temperatures ($>430^\circ\text{C}$); therefore, prior to high- k dielectric deposition, this surface oxide is not present, resulting in single crystalline ZrO deposition by ALD [26].

If a GeON surface layer is first formed, however, then this interfacial layer remains, resulting in amorphous ZrO film. Achieving improved pMOS devices with Ge wafers has been reported by several groups, but nMOS devices have not shown any improvement [25, 27]. One proposed explanation for this by Saraswat is the poor activation of n-type dopants in Ge material [25]. To avoid the Ge nMOS problem, Shang et al. proposed Ge SEG formation in pMOS device regions only by UHV CVD [27].

An alternative to Ge SEG is Ge-infusion directly into the channel region. This led to improvements to the ALD HfSiO gate leakage by a factor of two from 0.07A/cm^2 to 0.04A/cm^2 , or EOT reduction from 1.46nm to 1.28nm, along with good pMOS device characteristics but poor nMOS device characteristics. Ge-infusion can also solve the dopant activation problem for nMOS Ge devices. By using the replacement gate mask flow, Ge-channels can be formed directly in the nMOS channel regions, avoiding the nSDE and nS/D regions (Fig. 8).

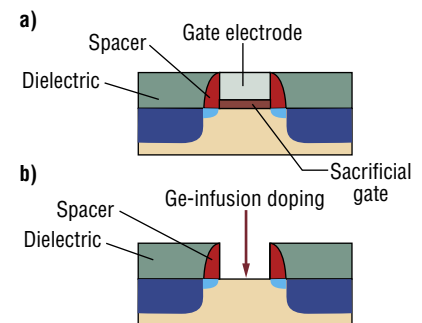


Figure 8. nMOS Ge-channel formation by Ge-infusion processing with replacement gate mask flow.

Conclusion

SiON gate dielectrics can be scaled to the sub-45nm node with an EOT of 0.7nm while maintaining gate leakage $<100 \text{A/cm}^2$ for HP logic devices. LSTP logic devices will start to use Hf-based dielectrics at the 65nm node, though devices using SiON with nitrogen content $>30\%$ could delay the switch until the 45nm node. LOP logic devices will extend SiON to the 45nm node.

Success in using these dielectric materials depends on 1) precise interface and interfacial layer control and 2) precise film deposition and compositional control. To accomplish these goals requires full-wafer metrology mapping techniques that provide quick chemical and electrical characterization of dielectric films and interfacial lay-

ers. Techniques such as using XPS for compositional and multilayer film thickness analysis and EM-probe measurement for gate leakage are needed.

It was observed that film compositional uniformity is key in realizing across-wafer device electrical uniformity. For Hf-based dielectrics, MOCVD HfSiON may be short-lived and used for only one or two nodes at the 65nm or 45nm node, while ALD and AVD Hf-rich dielectrics can be extended well beyond the 22nm node with the compositional uniformity and control needed to engineer the k value between 20–26, and gate leakage reduction by more than five orders-of-magnitude compared to SiO₂. Ge-infusion doping for pMOS SiGe SDE formation with compressive channel strain and direct Ge-channel formation for Ge CMOS devices could provide the channel mobility improvements needed for continued scaling — without the problems of using Ge wafers for CMOS devices below the 45nm node. ■

Acknowledgment

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JOHN BORLAND is the founder of *J.O.B. Technologies*, 5 Farrington Ln., South Hamilton, MA 01982.

EMIR GURER is director of applications at ReVera Inc. **MARK BENJAMIN** is applications lab manager at Solid State Measurements Inc. **WES SKINNER** is VP of marketing and sales at Epion Corp., e-mail wskinner@epion.com. **TOM SEIDEL** is EVP/CTO at Genus Inc. **MARCUS SCHUMACHER** is head of technology development at Aixtron AG.

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